



06/29/04

RW

Docket No. BUR920030023US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: Inventor(s): Clarence R. Ogilvie, Randall R. Pratt and Sebastian T. Ventrone
Title: METHOD AND APPARATUS FOR MEMORY ALLOCATION
Serial No.: 10/605,591
Filed: October 10, 2003

Transmitted herewith is:

☒ PTO Form 1449 and Information Disclosure Statement with twelve cited references.☒ Return Postcards

FEE CALCULATION

Fee Items	Claims Filed	Included With Basic Fee	Extra Claims	Fee Rate	Total
Total Claims	N/A	- 20 =	-0-	X \$18.00	\$0.00
Independent Claims	N/A	- 3 =	-0-	X \$84.00	\$0.00
Basic Filing Fee				\$740.00	\$0.00
TOTAL FEES					\$0.00

___ The Commissioner is hereby authorized to charge \$0.00 to Deposit Account No. 04-1696.

XX The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 04-1696. A duplicate copy of this transmittal is enclosed.

XX Please address all future correspondence to: **Brian M. Dugan**
Dugan & Dugan, PC
55 South Broadway
Tarrytown, NY 10591

I hereby certify that this correspondence is being deposited with the United States Postal Service as express mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Express Mail Receipt No. EV403025387USDate of Deposit: 6/28/04Signature: [Signature]

Respectfully submitted,

[Signature]
Brian M. Dugan
Registration No. 41,720
(914) 332-9081



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PATENTS
BUR920030023US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) : Clarence R. Ogilvie, Randall R. Pratt and
Sebastian T. Ventrone

Serial No. : 10/605,591

Filed : October 10, 2003

For : METHOD AND APPARATUS FOR MEMORY ALLOCATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97,
applicants wish to call the attention of the Examiner to the
following references:

U.S. Patent No. 4,729,090, Baba

U.S. Patent No. 5,218,680, Farrell et al.

U.S. Patent No. 5,218,686, Thayer

U.S. Patent No. 5,274,795, Vachon

Foreign Art Reference No. JP 61123969A (Japan)

Foreign Art Reference No. JP 60160459A (Japan)

Foreign Art Reference No. JP 61143863A (Japan)

United States Patent Application Pub. No.: US
2002/0129184 A1, Pub. Date: September 12, 2002.

K. Hwang, et al., "OMP: A RISC-based Multiprocessor
using Orthogonal-Access Memories and Multiple Spanning Buses*",
Laboratory for Parallel and Distributed Computing, University of
Southern California, Los Angeles, CA 90089 1990, pps. 7-22.

Ewert et al., "Optimizing Software Performance for IP
Frame Reassembly in an Integrated Architecture", WOSP 2000,
Ontario, Canada, pps. 29-37.

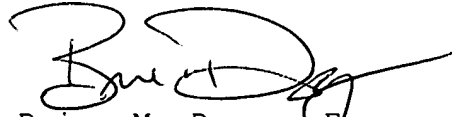
D.J. Schuelka, IBM Technical Bulletin, "Master/Slave
Cascade Channel for Microprocessor DMA", IBM Corp. 1979, Vol. 22,
No. 5, pps. 2041-2042.

IBM Technical Bulletin, "Multiword Direct Memory Access
Integrated Drive Electronics Hogpen", Vol. 39, No. 04, April
1996, pps. 203-206.

These references are also listed on the accompanying
Information Disclosure Statement (Form PTO-1449).

Consideration of the foregoing in relation to this
patent application is respectfully requested.

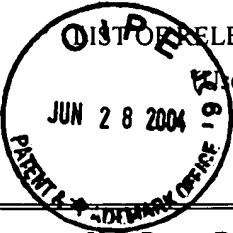
Respectfully Submitted,

A handwritten signature in black ink, appearing to read "Brian M. Dugan", with a stylized flourish extending from the end.

Brian M. Dugan, Esq.
Registration No. 41,720
Dugan & Dugan, PC
Attorneys for Applicants
(914) 332-9081

Dated:

6/28/04
Tarrytown, New York

U.S. Department of Commerce, Patent and Trademark Office <div style="text-align: center;">  </div>				Docket No.: BUR920030023US1		Serial No.: 10/605,591	
RELEVANT ART CITED BY APPLICANT (Use several sheets if necessary)				Applicants: Clarence R. Ogilvie et al.			
				Filing Date: October 10, 2003		Group: 	

U.S. Patent Documents							
*Examiner Initial	Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate	
	US-1	4,729,090	Baba				
	US-2	5,218,680	Farrell et al.				
	US-3	5,218,686	Thayer				
	US-4	5,274,795	Vachon				
	US-5						
	US-6						

Foreign Patent Documents							Translation	
	Document Number	Date	Country	Class	Subclass	Yes	No	
F-1	JP 61123969A	06/11/86	Japan			X <small>abstract only</small>		
F-2	JP 60160459A	08/22/85	Japan			X <small>abstract only</small>		
F-3	JP 61143863A	07/01/86	Japan			X <small>abstract only</small>		
F-4								
F-5								

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
OT-1	United States Patent Application Pub. No.: US 2002/0129184 A1, Pub. Date: September 12, 2002
OT-2	K. Hwang, et al., "OMP: A RISC-based Multiprocessor using Orthogonal-Access Memories and Multiple Spanning Buses*", Laboratory for Parallel and Distributed Computing, University of Southern California, Los Angeles, CA 90089 1990, pps. 7-22
OT-3	Ewert et al., "Optimizing Software Performance for IP Frame Reassembly in an Integrated Architecture", WOSP 2000, Ontario, Canada, pps. 29-37
OT-4	D.J. Schuelka, IBM Technical Bulletin, "Master/Slave Cascade Channel for Microprocessor DMA", IBM Corp. 1979, Vol. 22, No. 5, pps. 2041-2042
OT-5	IBM Technical Bulletin, "Multiword Direct Memory Access Integrated Drive Electronics Hogpen", Vol. 39, No. 04, April 1996, pps. 203-206

Examiner	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.